One-week Online Short-Term Training Program

on

"Emerging Nanoscale Devices, Circuits, and Its Applications" (NANODC-21)

Duration: May 10-14, 2021.

Coordinator – Dr. Sumit Kale, Assistant Professor, Department of ECE, DTU
Co-coordinator- Mr. Sachin Dhariwal, Assistant Professor, Department of ECE, DTU

ORGANIZING COMMITEE

Patron
Prof. Yogesh Singh
Vice Chancellor, DTU Delhi

Convenor
Prof. N S Raghava
HOD, ECE Dept., DTU Delhi

Coordinator
Dr. Sumit Kale
Assistant Professor
ECE Dept., DTU Delhi

Co-Coordinator
Mr. Sachin Dhariwal
Assistant Professor
ECE Dept., DTU Delhi

ABOUT THE INSTITUTE

Delhi Technological University located in Delhi is a premier institution of Engineering and Technology in India. The university plays a key role in the national and global knowledge network, empowering India with the wings of knowledge and innovation. The university aims to imbibe a culture of methodical research and to develop a scientific temper for the integration of science, engineering and management. DTU has been ranked amongst the top institutions in multiple reputed national and international surveys.

ABOUT THE DEPARTMENT

The Department of Electronics and Communication Engineering has experienced considerable growth since its inception in 1976. The vision of the department is to focus on the incubation of innovations in the areas of electronic design/ fabrication, and communication technologies, which are needed to address the growing challenges of tomorrow. The overall aim is to harbor a sustainable, and continuously evolving scientific, technological and educational environment which is both internationally-adapted and industry relevant.

OBJECTIVE OF THE STTP

The aim of this STTP is to provide a deep insight about basic concepts, technology and advancement of Emerging Nanoscale Devices and Circuits. In addition, it explores various applications of nanoscale semiconductor devices for future computing and information processing devices and systems. It also focuses on the fundamentals of nanoscale device design, methodology and testing. It will further give impetus to the participants towards bringing out newer and efficient techniques. Moreover, this short-term training program explore this area, the future scope of the technology, the issues, the challenges, and research opportunities.

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Organized by

Department of Electronics and Communication Engineering

Delhi Technological University
Bawana Road, Shahbad, Daulatpur
Delhi-110042

TOPICS TO BE COVERED

- Organic Thin Film Solar Cell Technology
- Devices and Circuit for Neuromorphic/In-memory Computing
- High Performance Organic Transistor and Memory for Flexible Electronics Applications
- 2D Materials Based Gas Sensors
- Device-circuit interaction in NCFETs
- Reliability and security issues in VLSI circuits and systems
- Device Random Fluctuations in Nano-scale MOSFETs
- Techniques for Broadband circuit design
- GaN Based Power Amplifier Design
- Neuromorphic Computing: Mapping Neural Networks to Hardware
- Engineering Ga2O3 based nanostructures and thin-film for high-performance deep UV Photodetectors
- Emerging trends in Doping and Junction free transistors

RESOURCE PERSONS

- Prof. Satyabrata Jit, Dept. of Electronics Engineering, IIT (BHU)
- Dr. Jawar Singh, Dept. of Electrical Engineering, IIT Patna
- Dr. Mahesh Kumar, Dept. of Electrical Engineering, IIT Jodhpur
- Dr. Mahendra Sakare, Dept. of Electrical Engineering, IIT Ropar
- Dr. Shree Prakash Tiwari, Dept. of Electrical Engineering, IIT Jodhpur
- Prof. Anand Bulusu, Dept. of ECE, IIT Roorkee
- Dr. Ambika Prasad Shah, Dept. of Electrical Engineering, IIT Jammu
- Dr. Shubhankar Majumdar, Dept. of ECE, NIT Meghalaya
- Dr. Shubham Sahay, Dept. of Electrical Engineering, IIT Kanpur
- Dr. Aakash Bag, Dept. of Computing and Electrical Engineering, IIT Mandi
- Dr. Chitrakant Sahu, Dept. of Electronics & Comm. Engineering, MNIT Jaipur
- Dr. Kaushik Nayak, Dept. of Electrical Engineering IIT Hyderabad

REGISTRATION

This STTP is open to the faculty members of AICTE/ UGC approved Engineering Institutes/Universities / R&D Labs /Industry person/ PhD scholars/ post graduate and undergraduate students interested to know about the current status, scope and challenges about Emerging Nanoscale devices, Circuits and their applications.

The interested person should fill the Google form by clicking on the link below:
https://forms.gle/dDHWUo1DGL4NJr2RA

No Registration fee is required for attending this STTP.

Important Dates

Last date of registration: May 7, 2021
Confirmation to the participants: May 9, 2021

Address for Correspondence

Coordinator
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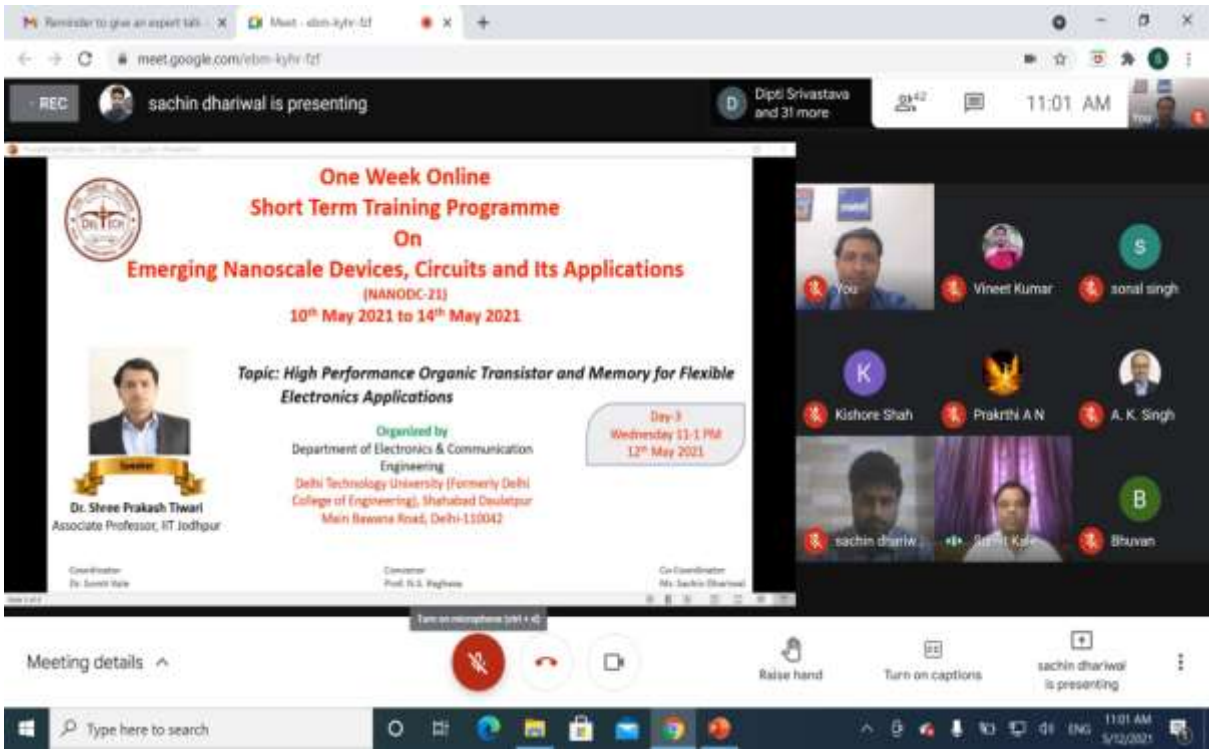
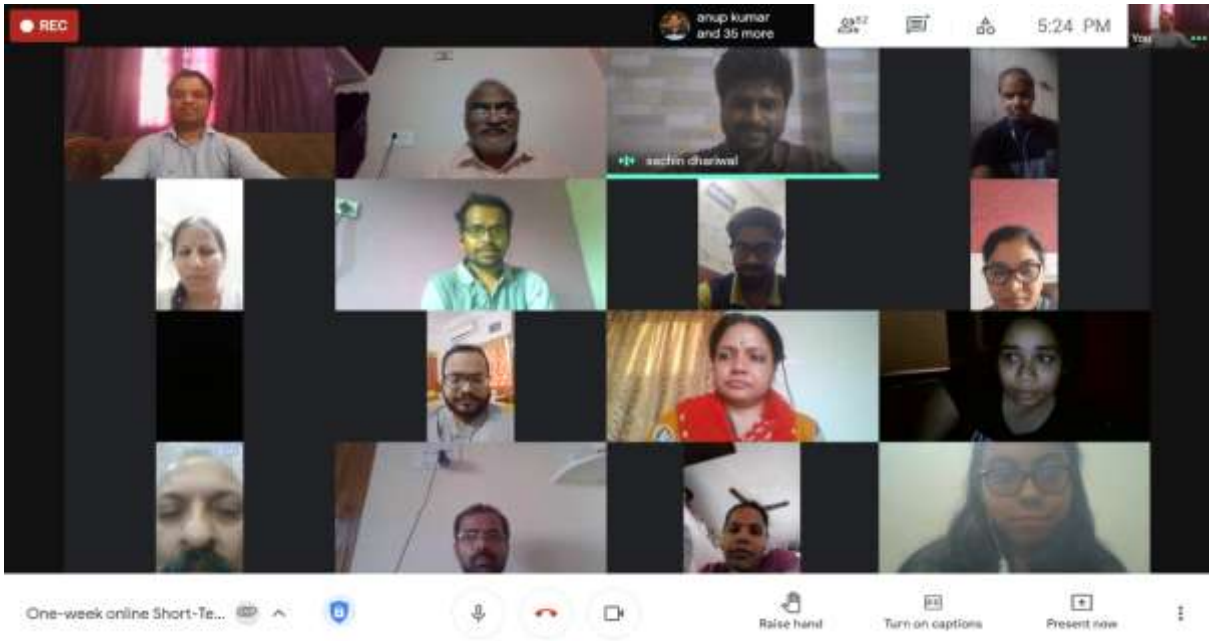
Phone: 09179417966, 09926337025

Co-Coordinator
Mr. Sachin Dhariwal
Assistant Professor
ECE Dept., DTU Delhi
Email: sachindhariwal@dtu.ac.in
Phone: 07737783332

Website: http://dtu.ac.in/
Note: E-Certificate will be provided to those participants whose attendance will be minimum 75% after successful completion of STTP.

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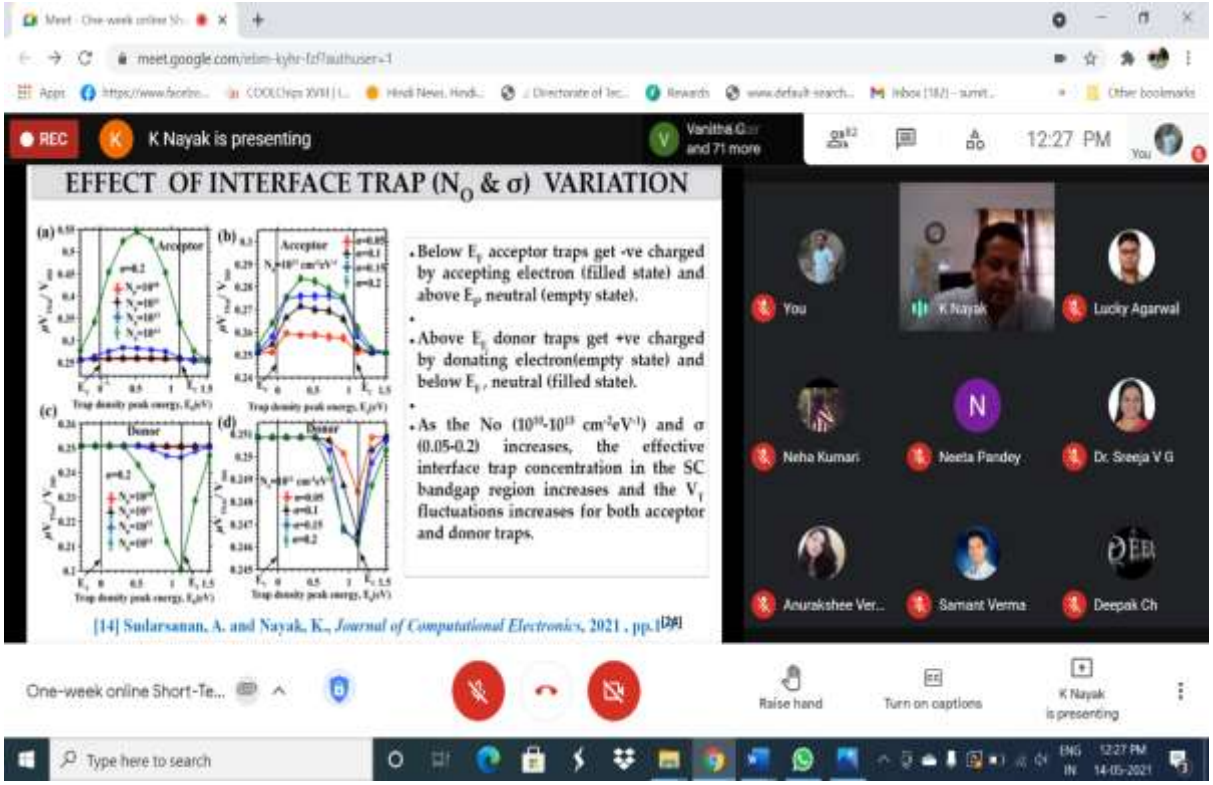
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K Nayak is presenting
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EFFECT OF INTERFACE TRAP (N_O & σ) VARIATION
Acceptor
Donor
Trap density peak energy, E_p(eV)
• Below E_V acceptor traps get -ve charged by accepting electron (filled state) and above E_p neutral (empty state).
• Above E_V donor traps get +ve charged by donating electron(empty state) and below E_p, neutral (filled state).
• As the No (10^{10}-10^{13} $cm^{-2}eV^{-1}$) and σ (0.05-0.2) increases, the effective interface trap concentration in the SC bandgap region increases and the V_t fluctuations increases for both acceptor and donor traps.
[14] Sudarsanan, A. and Nayak, K., Journal of Computational Electronics, 2021, pp.[2]
You
K Nayak
Lucky Agarwal
Neha Kumari
Neeta Pandey
Dr. Sreeja V G
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Samant Verma
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